Claims

What is claimed is:

1. A circuit comprising:

a subtractor coupled to receive a first input and a second input;

a multiplier coupled to a third input and an output of the subtractor;

an adder coupled to a fourth input and an output of the multiplier;

a first multiplexor whose output drives the first input;

a second multipexor whose output drives the second input;

a third multiplexor whose output drives the third input; and

a fourth multiplexor whose output drives the fourth input.

2. The circuit of claim 1 further comprising control logic configured to drive selection lines of the first, second, third and fourth multiplexors in response to a value in an operation register.

3. The circuit of claim 1, wherein, in response to a dynamic blending instruction in the operation register, the control logic is configured to drive the selection lines so that (a) the first multiplexor passes a color value of an image pixel to the first input, (b) the second multiplexor passes a color value of an accumulation buffer pixel to the second input, (c) the third multiplexor passes an alpha component of the image pixel to the third input, (d) the fourth multiplexor passes the color value of the accumulation buffer pixel to the fourth input.

4. The circuit of claim 1, wherein, in response to an add instruction in the operation register, the control logic is configured to drive the selection lines so that (a) the first multiplexor passes a component of an accumulation buffer pixel to the first input, (b) the second multiplexor passes a zero value to the second input, (c) the third multiplexor passes the value one to the third input, (d) the fourth multiplexor passes a bias value to the fourth input.

5. The circuit of claim 1, wherein, in response to an accumulate instruction in the operation register, the control logic is configured to drive the selection lines so that (a) the first multiplexor passes a component of an image pixel to the first input, (b) the second multiplexor passes a zero value to the second input, (c) the third multiplexor passes a scale value to the third input, (d) the fourth multiplexor passes a corresponding component of an accumulation buffer pixel to the fourth input.

6. The circuit of claim 1 further comprising an accumulator register, wherein an input line to the accumulator register couples to the output of the adder, wherein an output line of the accumulator register couples to an input of the fourth multiplexor.

7. The circuit of claim 1 wherein, in response to a matrix-oriented operation in the operation register, the control logic is configured to drive the selection lines so that (a) the first multiplexor passes the successive components of an input vector to the first input in successive cycles, (b) the second multiplexor passes the value zero to the second input in the successive cycles, (c) the third multiplexor passes corresponding matrix coefficients to the third input in the successive cycles, (d) the fourth multiplexor feeds back the output of the accumulator register to the fourth input in at least a subset of the successive cycles.

8. A system comprising:

a frame buffer containing an image buffer;

a texture buffer containing an accumulation buffer;

a pixel transfer unit comprising a control unit and one or more instances of a circuit, wherein the circuit comprises a subtractor, a multiplier, an adder, and a set of multiplexors, wherein the control logic drives select lines of the set of multiplexors in the one or more circuit instances through one or more computational cycles in order to implement a programmable operation, wherein the pixel transfer unit is configured to receive pixels values from one or more sources selected from a set of sources including the frame buffer and the texture buffer, wherein the pixel transfer unit is further

configured to implement the programmable operation on the pixel values using said one or more circuit instances to generate a stream of output pixels.

9. The system of claim 8, wherein the color depth precision of the accumulation buffer is larger than the color depth precision of the image buffer.

10. The system of claim 8 further comprising one or more circuit elements configured to transfer the stream of output pixels to a programmable destination.

11. The system of claim 10, wherein the programmable destination is the accumulation buffer.

12. The system of claim 10, wherein the programmable destination is the image buffer.

13. The system of claim 8, wherein the programmable operation includes one or more of an addition operation, a multiply operation, an accumulate operation, a dynamic blending operation, a matrix-vector multiplication, a load operation and a return operation.

14. The system of claim 13, wherein one or more of the circuit instances further includes an accumulator register for accumulating sums over multiple of said computational cycles.